AMENDMENTS TO THE SPECIFICATIONS

On page 1, please amend paragraph [03] as follows:

Conventional semiconductor devices comprise a semiconductor substrate, typically doped monocrystalline silicon, and a plurality of sequentially formed interlayer dielectrics and conductive patterns. An integrated circuit is formed containing a plurality of conductive patterns comprising conductive lines separated by interwiring spacings, and a plurality of interconnect lines, such as bus lines, bit lines, word lines and logic interconnect lines. Typically, the conductive patterns on different layers, i.e., upper and lower layers, are electrically connected by a conductive plug filling a via hole, while a conductive plug filling a contact hole establishes electrical contact with an active region on a semiconductor substrate, such as a source/drain region. Conductive lines are formed in trenches which typically extend substantially horizontal with respect to the semiconductor substrate. Semiconductor "chips" comprising five or more levels of metallization are becoming more prevalent as device geometry ~~shrink~~ shrinks to sub-micron levels.

Please amend paragraph [08] bridging pages 2 and 3 as follows:

In implementing Cu metallization, particularly in damascene techniques wherein an opening is formed in a dielectric layer, particularly a dielectric layer having a low dielectric constant, e.g., a dielectric constant less than about 3.9, various reliability, electromigration and resistance issues are generated. Reliability issues stem, in part, from the difficulty in forming a continuous seed layer on a barrier layer in an opening, particularly as the feature sizes continue to shrink into the deep sub-micron regime. For example, an opening is formed in dielectric layer 10, with barrier layer 11 lining the opening, as illustrated in Fig. 1. A seed layer 12 for deposition of Cu is then deposited by physical vapor deposition (PVD). As a result of reduced feature sizes and high aspect ratios, it is extremely difficult to deposit a continuous seed layer lining the sidewalls of the opening. Consequently, sidewall discontinuities in seed layer 12 form, as illustrated by reference numeral 13. In addition, it is even

difficult to effectively plate the seed layer 12 on the bottom of the opening. Cu cannot be electroplated on a discontinuous seed layer or where no seed layer exists. Consequently, voids are induced leading to high resistance vias and lines or open circuits.

On page 6, please amend paragraph [22] as follows:

[22] Thermal annealing in accordance with embodiments of the present invention enables a significant reduction ~~is~~ in resistivity, such as 40% to 60%, e.g. 50%, and a significant reduction in the average surface roughness (Ra) of the seed layer enhancement film, e.g., a reduction of up to 30% in the Ra. The seed layer enhancement film 20 is heated, as in nitrogen flowing at about rate of 2000 to about 20,000 sccm, resulting in the modified seed layer enhancement film 30 illustrated in Fig. 3. The improved seed layer enhancement film 30 exhibits a smoother surface and is thinned somewhat at the bottom and corners, thereby reducing contact resistance and improving filling. Thermal annealing drives out impurities, such as carbon, oxygen and hydrogen, thereby preventing subsequent voiding in the deposited Cu induced by outgassing during later processing.

On page 6, please amend paragraph [23] as follows:

Embodiments of the present invention comprise depositing a composite barrier layer of tantalum nitride and α-tantalum thereon, at an equivalent surface deposition thickness of about 100 Å to 400 Å, *i.e.*, the thickness on a wafer surface without topographical features, wherein the thickness of the composite barrier layer within the opening is about 7 Å to 40 Å. A PVD Cu seed layer is then deposited, such as at an equivalent surface deposition thickness of about 300 Å to 1,500 Å, e.g., 1,000 Å, wherein the thickness within the opening is of about 20 Å to about 100 Å. The conformal Cu seed layer enhancement film is then deposited and thermally annealed. The resulting Cu seed layer enhancement film has an aggregate carbon, nitrogen, oxygen and hydrogen impurity concentration no greater than 0.1 at .%.

On page 6, please amend paragraph [24] as follows:

The resistivity of the deposited seed layer enhancement film may be reduced from a deposited value of 2.5 to 6 microOhms-cm to an annealed value of 2.0 to 3 microOhm-cm. The average surface roughness (Ra) of the deposited seed layer enhancement film may be reduced from a deposited value of ~~13 Å to 36 Å~~ up to 40 Å to an annealed value of 19 Å to 25 Å.

On page 10, please amend paragraph [40] as follows:

Subsequent copper deposition may take place in an alkaline bath within the same apparatus employed to deposit the seed layer enhancement film However, subsequent copper deposition is desireably implemented in an acid environment where plating ~~palting~~ rates are substantially higher than corresponding rates associated with alkaline plating baths. To this end, the semiconductor workpiece may be transferred to an apparatus wherein the workpiece is thoroughly rinsed with deionized water and then transferred to the placing apparatus. For example, a suitable copper bath comprises 170 g/l H_2SO_4, 17 g/l copper and 70 ppm chloride ions with optional organic additives to produce desired film characteristics and provide better filling of the recessed structures on the wafer surface. The organic additives may include levelers, brighteners, wetting agents and ductility enhancers.